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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/610,497	06/30/2003	James Stuart Wight	CMA-0009	5376

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TESTA, HURWITZ & THIBEAULT, LLP
HIGH STREET TOWER
125 HIGH STREET
BOSTON, MA 02110

EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/610,497	WIGHT ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on June 30, 2003. Claims 1-13 are current pending.

Claim Rejections - 35 USC § 101 & 112

1. Claims 3,5,8,11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, and under 35 USC 101

Under 35 USC 112, second paragraph, meaning and scope of the claims 3,5,8 and 11 are unclear and indefinite since it merely recites a used without any active, positive steps delimiting how this use is actually practiced. Under 35 USC 101, the claims are not proper process claim as defined under 35 USC 101 (see MPEP 2173.05(q).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this vor a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (Figs 1-2, present specification pages 2-3; paragraphs 0002-0006).

Applicant's admitted prior art teaches an integrated circuit package, a method, and the use thereof, comprising, re claim 1, an integrated circuit die (10 in Fig 1; 24 in Fig 2, paragraph 0004) having at least one circuit etched thereon (paragraph 0005); and a housing (Fig 1, paragraph 0004 for printed circuit board, pad 22 with leads 16 as housing; and Figs 2-4, for board 52 with carrier pad 46; paragraphs 0004-0005) containing said integrated circuit die 10,24, wherein the integrated circuit die 10,24 is electrically coupled to the housing using at

least one wire bonds (14 in Fig 1; 28 in Fig 2; paragraph 0004); and wherein the at least wire bonds inherently have an inductance associated therewith (paragraph 0006); and wherein the wire bond inductance is used to facilitate operation of the at least one circuit as the wire bonds are electrically coupled to the circuits formed in the die and generate an amount of inductance during operation. Re further claim 2, as described above to claim 1, Applicant's admitted prior art discloses a method comprising of making available wire bonds 14,28 for electrically connected to circuit formed in the die, wherein the wire bonds 14,28 generate an amount of inductance during operation of the circuits (paragraph 0006), so that inductance of the wire bonds 14,28 are used to facilitate operation of a circuit contained in an integrated circuit package comprising making available wire bond inductance to the circuit from the wire bonds 14,28. Re claim 3, as described above to claims 1-2, Applicant's admitted prior art discloses using wire bonds 14,28, which are generating wire bond inductance during operation, in an integrated circuit package to facilitate operation of a circuit contained in an integrated circuit package, as the made wire bonds 14,28 are electrically connected to circuit formed in the die 10,24, wherein the wire bonds 14,28 generate an amount of inductance during operation (paragraph 0006). Re claims 4-5, wherein, as described above to claim 1, the circuit is contained in an integrated circuit die 10,24 housed in the integrated circuit package (Figs 1-2, paragraphs 0004-0005).

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Busking et al (6,107,684).

Busking et al teach an integrated circuit package, a method, and the use thereof, comprising, re claim 1, an integrated circuit die 5 (Figs 2-4; col 2, line 53 through col 4) having at least one circuit etched thereon (col 1, lines 15-33), and wherein the circuit also includes a on-die component 8 of bond wires (Fig 3B; col 3, lines 20-35); and a housing 11 containing said integrated circuit die 5 (col 2, lines 53-67; col 3, lines 1-14), wherein the integrated circuit die 5 is electrically coupled to the housing using at least one wire bonds 4,6,8 (Figs 1A-4B); and wherein the at least wire bonds have an inductance associated therewith (col 3, lines 50-60; line 28 through col 4; Figs 5,1A-4B); and wherein the wire bond inductance is used to facilitate operation of the at least one circuit as the wire bonds are electrically coupled to the circuits

formed in the die and generate an amount of inductance during operation. Re further claim 2, as described above to claim 1, Busking discloses a method comprising of making available wire bonds 4,6,8 for electrically connected to circuit formed in the die 5, wherein the wire bonds 4,6,8 generate an amount of inductance during operation of the circuits, so that inductance of the wire bonds are used to facilitate operation of a circuit contained in an integrated circuit package comprising making available wire bond inductance to the circuit from the wire bonds (Figs 5, 1A-4A, col 3, line 15 through col 4). Re claim 3, as described above to claims 1-2, Busking discloses using wire bonds 4,6,8 which are generating wire bond inductance during operation, in an integrated circuit package to facilitate operation of a circuit contained in an integrated circuit package, as the made wire bonds 4,6,8 are electrically connected to circuit formed in the die 5, wherein the wire bonds generate an amount of inductance during operation (Figs 5, 1A-4B, col 3, lines 15 through col 4). Re claims 4-5, wherein, as described above to claim 1, the circuit is contained in an integrated circuit die 5 housed in the integrated circuit package (Figs 1A-4B, col 2, line 53 through col 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 6-8 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Figs 1-2, present specification pages 2-3; paragraphs 0002-0006), in view of Tamura et al (6,166,971).

Applicant's admitted prior art teaches the integrated circuit package, the method, and the use thereof, as applied to claims 1-5 above and repeated herein, wherein an integrated circuit die has at least one circuit etched thereon (10 in Fig 1; 24 in Fig 2, paragraphs 0002-0005).

Applicant's admitted prior art does not teach the circuit comprising an impedance inverter (as recited in claims 6,7, and 8), or the circuit comprising a discrete filter as recited in claims 9, 10, and 11).

However, Tamura teaches an integrated circuit die comprising a driver circuit for correctly transmitting signals without waveform distortion (col 1, lines 6-20; line 64 through col 2) , wherein the circuit comprises a discrete filter (col 2, lines 4-13), and wherein the circuit comprises an impedance inverter (col 12, lines 20-35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Applicant's admitted prior art by forming at least one circuit comprised of a discrete filter and impedance inverter as taught by Tamura. This is at least because of the desirability to correctly transmit signals without waveform distortion or interference during operation of the integrated circuit die.

7. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Figs 1-2, present specification pages 2-3; paragraphs 0002-0006) in view of Van Roosmalen (5,844,301) or Leung et al (5,563,762).

Applicant's admitted prior art teaches the integrated circuit package, the method, and the use thereof, as applied to claims 1-5 above and repeated herein, wherein an integrated circuit die has at least one circuit etched thereon (10 in Fig 1; 24 in Fig 2, paragraphs 0002-0005).

Applicant's admitted prior art does not teach the circuit comprising on-die and off-die components

However, Van Roosmalen teaches (at col 1, lines 17-34) forming an integrated circuit die having at least one circuit, wherein at least one circuit comprises on-die and off-die components.

Leung teaches (at col 6, lines 35-47) forming an integrated circuit die having at least one circuit, wherein at least one circuit comprises on-die and off-die components.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Applicant's admitted prior art by forming the at least one circuit comprising on-die and off-die components as taught by Van Roosmalen or Leung. This is because of the desirability to largely reduce in system size of the integrated circuit package as some of the components are formed on the chip.

8. Claims 6-8 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busking et al (6,107,684) and further of Tamura et al (6,166,971).

Busking et al teach the integrated circuit package, the method, and the use thereof, as applied to claims 1-5 above and repeated herein, wherein an integrated circuit die 5 has at least one circuit etched thereon (Figs 1A-5; col 1, lines 15-33).

Busking et al do not teach the circuit comprising an impedance inverter (as recited in claims 6,7, and 8), or the circuit comprising a discrete filter as recited in claims 9, 10, and 11).

However, Tamura teaches an integrated circuit die comprising a driver circuit for correctly transmitting signals without waveform distortion (col 1, lines 6-20; line 64 through col 2) , wherein the circuit comprises a discrete filter (col 2, lines 4-13), and wherein the circuit comprises an impedance inverter (col 12, lines 20-35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Busking by forming at least one circuit comprised of a discrete filter and impedance inverter as taught by Tamura. This is at least because of the desirability to correctly transmit signals without waveform distortion or interference during operation of the integrated circuit die.

9. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busking (6,107,684) in view of Van Roosmalen (5,844,301) or Leung et al (5,563,762).

Busking et al teach the integrated circuit package, the method, and the use thereof, as applied to claims 1-5 above and repeated herein, wherein an integrated circuit die 5 has at least

one circuit etched thereon (Figs 1A-5; col 1, lines 15-33), and wherein the circuit includes a on-die component 8 (Fig 3B; col 3, lines 20-35).

Busking et al do not teach the circuit comprising on-die and off-die components

However, Van Roosmalen teaches (at col 1, lines 17-34) forming an integrated circuit die having at least one circuit, wherein at least one circuit comprises on-die and off-die components. Leung teaches (at col 6, lines 35-47) forming an integrated circuit die having at least one circuit, wherein at least one circuit comprises on-die and off-die components.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Busking by forming the at least one circuit comprising on-die and off-die components as taught by Van Roosmalen or Leung. This is because of the desirability to largely reduce in system size of the integrated circuit package as some of the components are formed on the chip.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-3

Michael Trinh
Primary Examiner